

This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS ✓
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

**As rescanning documents *will not* correct images,
please do not report the images to the
Image Problem Mailbox.**

1 CLAIMS:

2 1. A method of fabricating integrated circuitry comprising:
3 forming a conductive line having opposing sidewalls over a
4 semiconductor substrate;
5 depositing an insulating layer over the substrate and the line;
6 etching the insulating layer proximate the line along at least a
7 portion of at least one sidewall of the line; and
8 after the etching, depositing an insulating spacer forming layer
9 over the substrate and the line, and anisotropically etching it to form
10 an insulating sidewall spacer along said portion of the at least one
11 sidewall.

12
13 2. The method of claim 1 wherein the etching of the insulating
14 layer is conducted along at least a portion of each of the opposing line
15 sidewalls, the anisotropic etching forming an insulating sidewall spacer
16 over each of the opposing line sidewalls.

17
18 3. The method of claim 1 wherein the etching of the insulating
19 layer is conducted along the portion of the one sidewall and not along
20 the opposing sidewall.

21
22 4. The method of claim 1 wherein the portion comprises a
23 majority of said one sidewall.
24

1 5. The method of claim 1 wherein the portion comprises the
2 substantial entirety of said at least one sidewall.

3
4 6. The method of claim 1 wherein the etching of the insulating
5 layer outwardly exposes material of the semiconductor substrate.

6
7 7. The method of claim 1 wherein the conductive line is
8 formed to comprise a transistor gate.

9
10 8. The method of claim 1 comprising planarizing the insulating
11 layer prior to said etching of it.

12
13 9. The method of claim 1 comprising:
14 forming field isolation material regions and active area regions on
15 the semiconductor substrate before the depositing;
16 etching a trench into the field isolation material and the insulating
17 layer into a desired local interconnect line configuration; and
18 forming a local interconnect layer of material over the substrate
19 which at least partially fills the trench and which electrically connects
20 with one of the active area regions.

1 10. A method of fabricating integrated circuitry comprising:
2 forming a pair of transistor gates having respective opposing
3 sidewalls over a semiconductor substrate, one sidewall of one of the
4 transistor gates facing one sidewall of the other transistor gate;
5 depositing an insulating layer over the substrate and between the
6 pair of transistor gates to fill an area extending therebetween;
7 etching a contact opening into the insulating layer to proximate
8 the substrate between the pair of transistor gates;
9 depositing an insulating spacer forming layer within the contact
10 opening to less than completely fill the contact opening; and
11 anisotropically etching the spacer forming layer to form a pair of
12 insulating sidewall spacers over the one sidewalls of the pair of
13 transistor gates.

14
15 11. The method of claim 10 wherein the contact opening etching
16 exposes material of the semiconductor substrate.

17
18 12. The method of claim 10 wherein the contact opening etching
19 exposes conductive material of at least one of the pair of transistor
20 gates.

21
22 13. The method of claim 10 wherein the contact opening etching
23 exposes conductive material of each of the pair of transistor gates.
24

1 14. The method of claim 10 wherein the contact opening etching
2 exposes conductive material of at least one of the sidewalls of at least
3 one of the pair of transistor gates.

4
5 15. The method of claim 10 comprising planarizing the insulating
6 layer prior to said etching of it.

7
8 16. The method of claim 10 comprising:
9 forming field isolation material regions and active area regions on
10 the semiconductor substrate before the depositing;
11 etching a trench into the field isolation material and the insulating
12 layer into a desired local interconnect line configuration; and
13 forming a local interconnect layer of material over the substrate
14 which at least partially fills the trench and which electrically connects
15 with one of the active area regions.

1 17. A method of fabricating integrated circuitry comprising:
2 forming a pair of transistor gates having respective opposing
3 sidewalls over a semiconductor substrate, one sidewall of one of the
4 transistor gates facing one sidewall of the other transistor gate;
5 depositing an insulating layer over the substrate and between the
6 pair of transistor gates to fill an area extending therebetween;
7 etching a contact opening into the insulating layer to proximate
8 the substrate between the pair of transistor gates, the etching exposing
9 conductive material of at least one of the one sidewalls of the pair of
10 transistor gates;
11 after the etching, covering the at least one of the one sidewalls
12 with insulating material; and
13 forming electrically conductive material within the opening in
14 electrical connection with material of the semiconductor substrate.
15
16 18. The method of claim 17 wherein the contact opening etching
17 exposes conductive material of each of the one sidewalls of each of the
18 pair of transistor gates.
19
20 19. The method of claim 17 wherein the covering comprises
21 deposition of an insulating layer.
22
23
24

1 20. The method of claim 17 wherein the covering comprises
2 deposition of an insulating layer, and subsequent anisotropic etching
3 thereof.

4
5 21. The method of claim 17 comprising planarizing the insulating
6 layer prior to the contact opening etching.

7
8 22. The method of claim 17 comprising:
9 forming field isolation material regions and active area regions on
10 the semiconductor substrate before the depositing;
11 etching a trench into the field isolation material and the insulating
12 layer into a desired local interconnect line configuration; and
13 forming a local interconnect layer of material over the substrate
14 which at least partially fills the trench and which electrically connects
15 with one of the active area regions.

1 23. A method of forming a local interconnect comprising:
2 forming a pair of transistor gates having respective opposing
3 sidewalls over a semiconductor substrate;
4 depositing an insulating layer over the substrate and between the
5 pair of transistor gates;
6 etching a first contact opening into the insulating layer to
7 proximate the substrate between the pair of transistor gates and another
8 contact opening through the insulating layer to proximate the substrate
9 proximate an opposing side of one of the pair of transistor gates;
10 forming insulating sidewall spacers over the opposing sidewalls of
11 the one transistor gate, the insulating layer being received between at
12 least one of said sidewalls and one of said sidewall spacers; and
13 forming a local interconnect layer to overlie the one transistor
14 gate and electrically connect with semiconductor substrate material
15 between the pair of transistor gates and semiconductor substrate material
16 proximate the opposing side of the one transistor gate.

17
18 24. The method of claim 23 wherein the insulating layer is not
19 received between the other sidewall and the other sidewall spacer.

20
21 25. The method of claim 23 wherein the etching exposes
22 material of the semiconductor substrate within the first and another
23 contact openings.
24

1 26. The method of claim 23 comprising planarizing the insulating
2 layer prior to said etching of it.

3
4 27. The method of claim 23 wherein the insulating layer as
5 received between the one sidewall and the one sidewall spacer has a
6 maximum lateral thickness which is greater than or equal to a maximum
7 lateral thickness of the one sidewall spacer.

8
9 28. The method of claim 23 wherein the local interconnect layer
10 comprises polysilicon.

11
12 29. The method of claim 23 comprising:
13 forming field isolation material regions and active area regions on
14 the semiconductor substrate before the depositing;
15 etching a trench into the field isolation material and the insulating
16 layer into a desired local interconnect line configuration; and
17 forming the local interconnect layer to at least partially fill the
18 trench and which electrically connects with one of the active area
19 regions.

1 30. A method of forming a conductive line comprising:
2 forming conductive material received over a semiconductor
3 substrate into a line, the line having opposing sidewalls;
4 depositing insulative material over the line and etching it to be
5 received over one of the opposing sidewalls and not the other;
6 depositing an insulating spacer forming layer over the line and the
7 etched insulative material; and
8 anisotropically etching the spacer forming layer to form a pair of
9 insulative spacers over the opposing line sidewalls, the insulative material
10 being received between the one sidewall and one insulative spacer
11 formed thereover and not being received between the other sidewall and
12 the other spacer formed thereover.

13
14 31. The method of claim 30 comprising planarizing the insulating
15 layer prior to said etching of it.

16
17 32. The method of claim 30 wherein the insulative material as
18 received between the one sidewall and the one sidewall spacer formed
19 thereover has a maximum lateral thickness which is greater than or
20 equal to a maximum lateral thickness of the one sidewall spacer.

1 33. A method of forming a conductive line comprising:
2 forming conductive material received over a semiconductor
3 substrate into a line, the line having opposing sidewalls;
4 depositing insulative material over the line;
5 planarizing the insulative material;
6 depositing an insulating spacer forming layer over the line and the
7 planarized insulative material; and
8 anisotropically etching the spacer forming layer to form a pair of
9 insulative spacers over the opposing line sidewalls, the insulative material
10 being received between at least one of the sidewalls and one insulative
11 spacer formed thereover.

12
13 34. The method of claim 33 wherein the insulative material as
14 received between the one sidewall and the one sidewall spacer formed
15 thereover has a maximum lateral thickness which is greater than or
16 equal to a maximum lateral thickness of the one sidewall spacer.

1 35. A method of forming a local interconnect comprising:
2 forming at least two transistor gates over a semiconductor
3 substrate;

4 depositing a local interconnect layer to overlie at least one of the
5 transistor gates and interconnect at least one source/drain region of one
6 of the gates with semiconductor substrate material proximate another of
7 the transistor gates;

8 implanting conductivity enhancing impurity into the local
9 interconnect layer in at least two implanting steps, one of the two
10 implantings providing a peak implant location which is deeper into the
11 layer than the other; and

12 diffusing conductivity enhancing impurity from the local
13 interconnect layer into semiconductor substrate material therebeneath.

14
15 36. The method of claim 35 comprising conducting the one
16 implanting relative to one portion of the local interconnect layer to
17 have a peak implant location which is through said layer and within the
18 semiconductor substrate material therebeneath.

19
20
21
22
23
24

1 37. A method of forming a local interconnect comprising:
2 forming at least two transistor gates over a semiconductor
3 substrate;

4 depositing a local interconnect layer to overlie at least one of the
5 transistor gates and interconnect at least one source/drain region of one
6 of the gates with semiconductor substrate material proximate another of
7 the transistor gates; and

8 implanting conductivity enhancing impurity through the local
9 interconnect layer into semiconductor substrate material therebeneath.
10

11 38. The method of claim 37 further comprising in another
12 implanting step separate from said implanting, implanting conductivity
13 enhancing impurity to a peak concentration location which is within the
14 local interconnect layer.
15
16
17
18
19
20
21
22
23
24

1 39. A method of fabricating integrated circuitry comprising:
2 forming a gate dielectric layer over a semiconductor substrate;
3 forming a conductively doped semiconductive layer over the gate
4 dielectric layer;
5 forming an insulative capping layer over the semiconductive layer;
6 forming an etch stop layer over the insulative capping layer;
7 patterning and etching the etch stop layer, the capping layer and
8 the semiconductive layer into a plurality of transistor gate lines;
9 depositing an oxide layer over the substrate and the transistor
10 gate lines to a thickness greater than that of the combined etched etch
11 stop layer, capping layer and semiconductor layer;
12 chemical mechanical polishing the deposited oxide layer using the
13 etch stop layer as an etch stop;
14 patterning and etching the polished oxide layer to expose material
15 of the semiconductor substrate in at least two discrete locations
16 proximate different of the plurality of gate lines;
17 depositing a local interconnect layer into electrical connection with
18 said locations and over said plurality of gate lines; and
19 etching the local interconnect layer into a local interconnect line
20 overlying at least two of said plurality of gate lines.
21
22
23
24

1 40. A method of forming a conductive line comprising:
2 forming field isolation material regions and active area regions on
3 a semiconductor substrate;
4 etching a trench into the field isolation material into a desired
5 line configuration; and
6 depositing a conductive material to at least partially fill the trench
7 and form a conductive line therein.

8
9 41. The method of claim 40 comprising forming the field
10 isolation material to comprise LOCOS oxide.

11
12 42. The method of claim 40 comprising depositing an insulative
13 layer over the active area and field isolation regions, and planarizing
14 the insulative layer prior to the etching.

15
16 43. The method of claim 40 comprising depositing an insulative
17 layer over the active area and field isolation regions, and planarizing
18 the insulative layer prior to the etching; the etching comprising etching
19 the trench to be received within the planarized insulative layer.

20
21 44. The method of claim 40 comprising forming the field
22 isolation material to comprise CVD oxide formed within etched substrate
23 trenches.

1 45. The method of claim 40 wherein the conductive material is
2 initially deposited to overfill the trench, and comprising removing some
3 of the conductive material after the initial deposition to leave the
4 trench only partially filled with the conductive material.

5
6 46. A method of forming a local interconnect comprising:
7 etching a trench into field isolation material formed relative to a
8 semiconductor substrate, the trench in the field isolation material
9 extending to an edge of the isolation material proximate active area
10 substrate material; and

11 forming a local interconnect layer of material over the substrate
12 which at least partially fills the trench and which electrically connects
13 with said active area substrate material.

14
15 47. The method of claim 46 comprising forming the field
16 isolation material to comprise LOCOS oxide.

17
18 48. The method of claim 46 comprising forming the field
19 isolation material to comprise CVD oxide formed within etched substrate
20 trenches.

1 49. The method of claim 46 wherein the local interconnect layer
2 is initially deposited to overfill the trench, and comprising removing
3 some of the interconnect layer after the initial deposition to leave the
4 trench only partially filled with the interconnect layer.

5
6 50. Integrated circuitry comprising:
7 a semiconductor substrate comprising field isolation material
8 regions and active area regions; and
9 a conductive line received within a trench formed within the field
10 isolation material.

11
12 51. The integrated circuitry of claim 50 wherein the field
13 isolation material comprises LOCOS oxide.

14
15 52. The integrated circuitry of claim 50 wherein the field
16 isolation material comprises CVD oxide formed within etched substrate
17 trenches.

18
19 53. The integrated circuitry of claim 50 wherein the conductive
20 line within the trench is defined by the shape of the trench formed
21 within the field isolation material.

22
23 54. The integrated circuitry of claim 53 wherein the field
24 isolation material comprises LOCOS oxide.

1 55. The integrated circuitry of claim 53 wherein the field
2 isolation material comprises CVD oxide formed within etched substrate
3 trenches.

4
5 56. The integrated circuitry of claim 50 wherein the trench has
6 opposing insulative sidewalls comprising the field isolation material,
7 conductive material of the line contacting the trench sidewalls.

8
9 57. Integrated circuitry comprising:
10 a semiconductor substrate comprising field isolation material
11 regions and active area regions; and
12 a local interconnect line extending from over and in electrical
13 connection with an active area region to within a trench formed within
14 the field isolation material.

15
16 58. The integrated circuitry of claim 57 wherein the field
17 isolation material comprises LOCOS oxide.

18
19 59. The integrated circuitry of claim 57 wherein the field
20 isolation material comprises CVD oxide formed within etched substrate
21 trenches.

1 60. The integrated circuitry of claim 57 wherein the conductive
2 line within the trench is defined by the shape of the trench formed
3 within the field isolation material.

4
5 61. The integrated circuitry of claim 60 wherein the field
6 isolation material comprises LOCOS oxide.

7
8 62. The integrated circuitry of claim 60 wherein the field
9 isolation material comprises CVD oxide formed within etched substrate
10 trenches.

11
12 63. The integrated circuitry of claim 60 wherein the trench has
13 opposing insulative sidewalls comprising the field isolation material,
14 conductive material of the local interconnect line contacting the trench
15 sidewalls.